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Information Disclosure Statement by Applicant	Applicant: Lea Di Cioccio, et al	
(Use several sheets if necessary)	Filed: March 2, 2005	Group: Unassigned

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
SB		5,880,491	03/09/1999	Soref et al.			
		6,328,796 B1	12/11/2001	Kub et al.			
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Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No
SB		02/43124 A2	05/30/2002	WO				
SB		2 774 214	07/30/1999	FR				

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

		International Search Report, FRANCE
SB		LETERTRE, F. ET AL., "QuaSiC Smart-Cut Substrates for SIC High Power Devices", Materials Science Forum, Aedermannsfdorf, CH, Vol. 389-393 10/28/2001 pages 151-154, XP008018649
SB		VINOD, K. N., ET AL., "Fabrication of Low Defect Density 3C-SiC on SiO_2 Structures Using Wafer Bonding Techniques", Journal of Electronic Materials, Warrendale, PA, US, vol. 27,no. 3, 03/1998, pages L17-L20, XP009003060
SB		NISHINO, S. ET AL., "Production of Large-Area Single-Crystal Wafers of Cubic SiC for Semiconductor Devices", Applied Physics Letters, American Institute of Physics. New York, US, vol. 42, no. 5, 03/01/1983, pages 460-462, XP000567924
SB		NEYRET, E. ET AL., "Deposition, Evaluation and Control of 4H and 6H SiC Epitaxial Layers for Device Applications", Material Science and Engineering B, Elsevier Sequoia Lausanne, CH, vol. 80, no. 1-3, 03/22/2001, pages 332-336, XP004234724

Examiner /Seth Barnes/	Date Considered 07/20/2006

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.